Pulsed Internal-Node Waveform Study of Flip-Chip MMIC Power Amplifiers

J. W. Bao, C. J. Wei and J. C. M. Hwang
Lehigh Univ., 5 E. Packer Av., Bethlehem PA 18015
R. F. Wang and C. P. Wen
Hughes Aircraft Co., 24210 Garnier St., Torrance CA 90509

Abstract—**A pulsed internal-node microwave waveform probing technique was developed and used to characterize flip-chip MMIC power amplifiers. Variations in load impedances were found across the band and different unit cells.**

INTRODUCTION

Typically, microwave amplifiers are tested under CW instead of pulsed conditions for simpler instrumentation and better signal-to-noise ratio. However, due to thermal degradation effects, MMIC power amplifiers that are designed for pulsed operations cannot be properly tested under CW conditions. This presents especially a dilemma for flip-chip amplifiers. On one hand, they would burn out if CW tested before flip-mounting on a heat sink. On the other hand, once mounted, they are no longer accessible. Even when pulsed test conditions are used, typically only the envelope function is measured thus leaving behind a wealth of information in the carrier waveform.

Recently, we have developed a novel internal-node waveform probing technique and reported its application to MMIC power amplifiers in CW operation [1]. We report in this paper, for the first time, the extension of such a technique to MMIC power amplifiers in pulsed operations. As the result, unprecedent insights were obtained for the operation of these amplifiers which insights can be used for model verification, design optimization, process diagnosis, and reliability assessment.

EXPERIMENTAL

As shown schematically in Fig. 1, the experimental setup is similar to that of [1] except that both the dc bias and RF input are simultaneously pulsed on and off using a pulse/function generator. This pulse/function generator also triggers a transition analyzer to sample the internal-node waveform measured via a high-impedance probe.

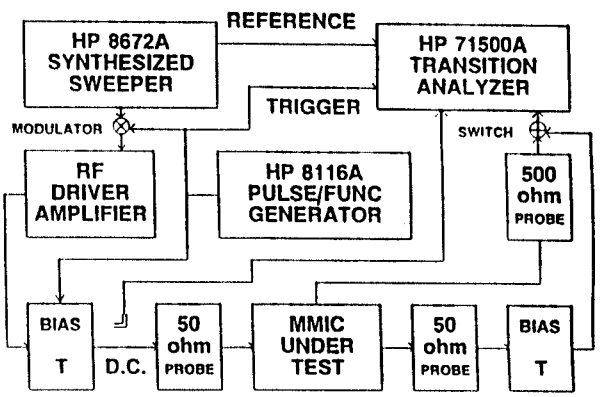

Fig. 1 Pulsed internal-node measurement setup.

The transition analyzer uses a harmonic sampling technique to acquire both the waveform in time domain and the harmonic magnitudes and phases in frequency domain. The phase is measured in reference to either the amplifier input or output waveform which is simultaneously measured on another channel of the transition analyzer. Frequency-domain calibration techniques

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are used to accurately rotate the measured waveforms from the transition analyzer to the internal node on the MMIC. From the voltage waveforms of two nodes that are separated by a known impedance such as a transmission line of know length and characteristic impedance, current waveforms are calculated. Dynamic load lines are then calculated from the current and voltage waveforms.

The waveforms are sampled at a rate of 20 MHz. Typically, 40 sampling points are used to acquire a waveform in 2 μs which is a reasonable compromise between the time and harmonic resolutions. A greater number of sampling points can be used to resolve weak harmonics but may miss very rapid transients. Using this technique, the internal-node as well as the output waveforms are monitored as a function of time after the amplifier is pulsed on.

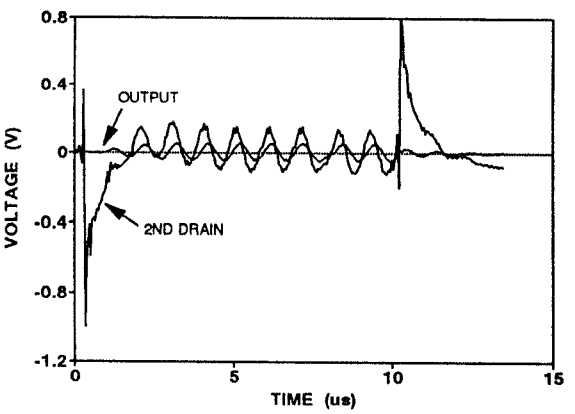


Fig. 2 As-measured waveforms at the amplifier output and the drain of one of the second-stage unit cells. *Pin* = 20 dBm @ 8 GHz.

The results presented in the following are measured on flip-chip MESFET X-band double-stage MMIC power amplifiers. The design is based on coplanar waveguides built on a 600 μm thick GaAs substrate without via-hole grounding. The first amplifier stage consists of two unit cells, whereas the second stage has four unit cells. Single gate and drain supplies are fed to both stages through bias distribution networks. To turn on the amplifier, the gate supply is pulsed from -5.5 to 0 V while the drain supply is held at 7 V. To minimize the thermal effect, the pulse width is typically 10 μs while the pulse rate is 200 Hz.

RESULTS AND DISCUSSION

Fig. 2 compares the as-sampled waveforms of the amplifier output with that of the drain of one of the second-stage cells. It can be seen that, while the amplifier output appears to be turned on and off smoothly, the second-stage drain actually undergoes very large transients which can be a reliability concern. The second-stage drain also contains more harmonics which appear to be filtered by the output matching circuit.

Notice that, while the as-sampled waveforms are representative of the carrier at 8 GHz in this case, the waveforms appear to have a period of the order of μs due to the aliasing effect of the sampling technique. Each period of the as-sampled waveform can be transformed into the frequency domain to analyze the evolution with time of its harmonic content. In the remainder of this paper we concentrate on waveforms measured at 5 μs after the amplifier is pulsed on.

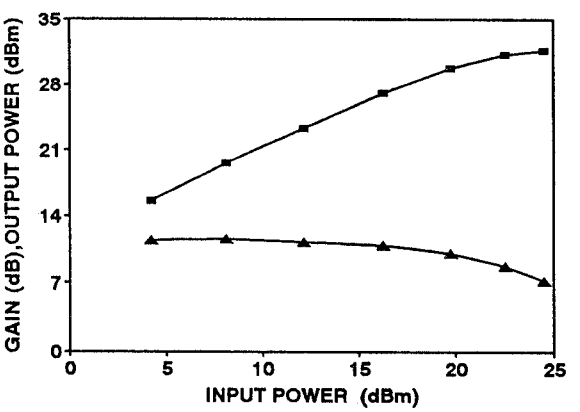


Fig. 3 10 GHz fundamental (▲) gain and (■) output power measured 5 μs after the amplifier is pulsed on.

Fig. 3 shows the 10 GHz fundamental gain and output power. The small-signal gain of 12 dB and the 1 dB compression power of 27 dBm are

comparable to that of a flip-mounted amplifier measured in the conventional manner with a duty factor as high as 30%. This suggests that gate-lag is not a concern and flip-mounting provide excellent heat sinking for these amplifiers.

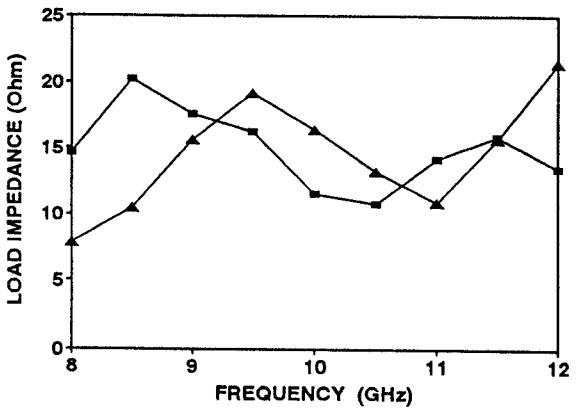
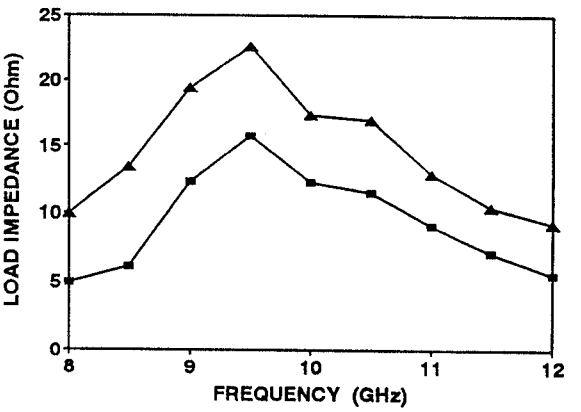


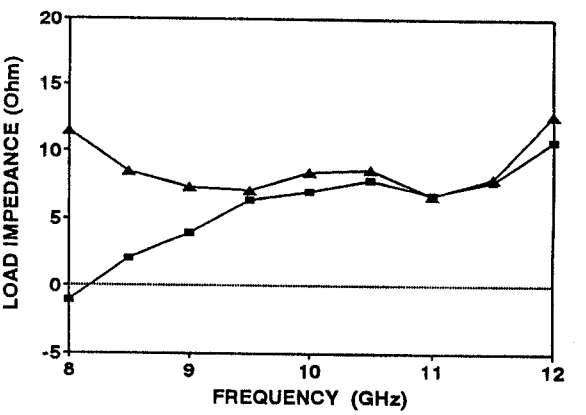
Fig. 4 (▲) Real and (■) imaginary parts of the load impedance of a first-stage unit cell. *Pin* = 10 dBm.

The load impedances measured from each of the two amplifier stages appear to be not too far off the design values. However, their variations across the band and across different unit cells are less than desirable. Fig. 4 shows the load impedance of one of the two first-stage cells measured under an input power of 10 dBm and 8 to 12 GHz. The results from both cells are very similar to each other. In each case, while both the real and imaginary parts of the load impedance vary significantly across the band, the dip in load resistance near the lower end of the band is of a particular concern because it can contribute to power roll off there.

For the four second-stage cells, the measured load impedance of the two inner cells are similar to each other, while that of the two outer cells are similar to each other. Fig. 5 compares the load impedance between an inner and an outer cell. Here while the real loads track each other across the band, the imaginary loads diverge toward the lower band edge. At 8 GHz, the load for the outer unit cell turns capacitive which is opposite to what is required for conjugate match, further aggravating the power roll off there. In addition, the imbalance between the inner and outer cells can cause odd-mode oscillations between the cells. Unlike the previous CW case [1], this imbalance is not thermally related hence probably due to imprecise passive-element modeling or layout variation.



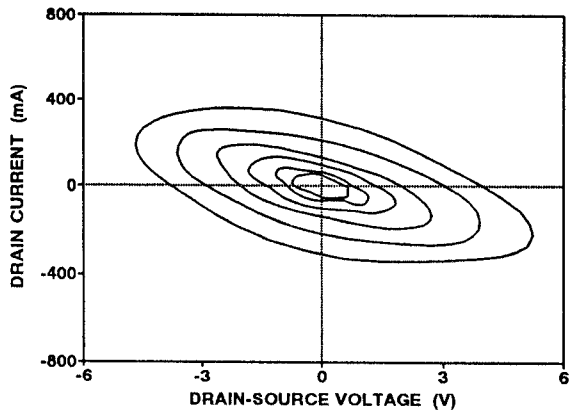
(a)



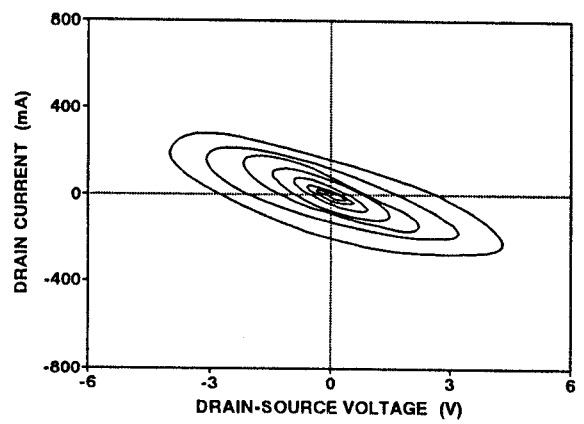
(b)

Fig. 5 (a) Real and (b) imaginary parts of the load impedance of an (▲) inner and (■) outer unit cell of the second stage. *Pin* = 10 dBm.

As the amplifier is driven into compression, similar imbalances are seen across the band and the cells. Fig. 6 compares the dynamic load lines of a first-stage cell at 8 and 9 GHz. Fig. 7 compares the dynamic load lines of an inner and an outer second-stage cell at 8 GHz.

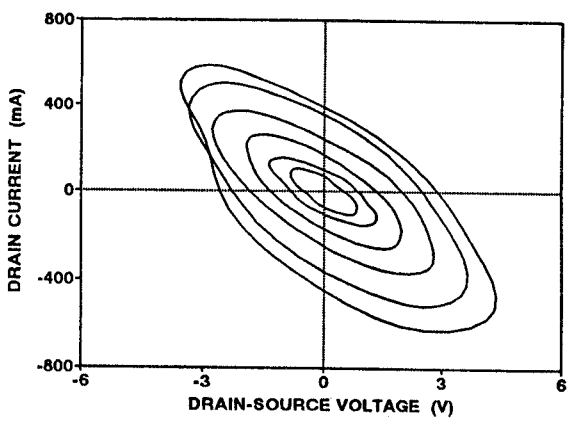


(a)

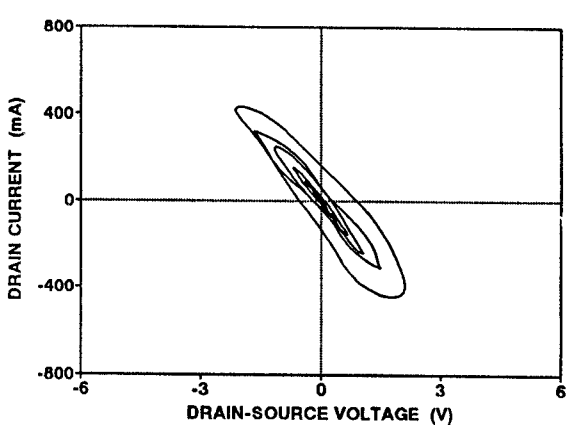


(b)

Fig. 6 Dynamic load lines of a first-stage cell. *Pin* = 4, 8, 12, 16, 19, and 22 dBm at (a) 8 and (b) 9 GHz.



(a)



(b)

Fig. 7 Dynamic load lines of an (a) inner and (b) outer second-stage cell. *Pin* = 4, 8, 12, 16, 19, and 22 dBm at 8 GHz.

CONCLUSION

In conclusion, we have developed a pulsed internal-node probing technique to obtain both the envelope and waveform information for MMIC power amplifiers in pulsed operations. The examples given above illustrate the broad impact of such a pulsed testing technique for MMIC model verification, design optimization, process diagnosis, and reliability assessment.

REFERENCES

[1] C. J. Wei, Y. A. Tkachenko, J. C. M. Hwang, K. R. Smith and A. H. Peake, "Internal-node waveform analysis of MMIC power amplifiers," *IEEE Trans. MTT-S*, vol. 43, pp. 3037-3042, Dec. 1995.

[2] C. P. Wen, W. D. Wong, C. K. Pao, J. L. Snopkowsi and D. L Ingram, "Coplanar waveguide based, dielectric coated flip chip monolithic microwave integrated circuit, a paradigm shift in MMIC technology" in *Dig. IEEE Microwave Millimeter-wave Monolithic Circuits Symp.*, May 1995, pp. 123-126.